Volume II, Section 5:
Validation Checklist (809)[1]
Q3500/Q5000/Q1400 Arrays

Those who do not study history, are bound to repeat it

[1] 1999, approximately. Matched the Q1400 Bipolar and Q5000 Arrays.

1 Design Validation for Arrays (809)

The logic design methodology required to successfully implement high-performance gate and logic arrays includes a complex sequence of checks and reviews. Structured design procedures must be followed carefully to avoid costly failures.

One aspect of structured design methodology is the design validation process. That process consists of a rigorous review of the logic design, themacros chosen, the interconnection scheme, and dozens of other considerations that experience has shown could detect such potential failures before they occur.

A design validation review is required for al designs done with the aid of the DAISY, MENTOR , and VALID systems[2] engineering workstations (EWS) or VAX/VMS-based LASAR 6 systems, whether the design workis performed by the customer or by AMCC Implementation Engineering.

The AMCC design validation software, part of the AMCC MACROMATRIX package and know as the Engineering Rules Checks (ERCs), is used to perform many of the necessary design checks and to create various output reports that both list the errors found and supply valuable design documentation to the user and to AMCC. ERC software is currently available on all AMCC-supported RWS systems and the VAX. [3]

In all cases, the process of reviewing the ERC output, and correcting the design to remove any discrepancies, helps to ensure that the circuit will be build-able and testable.

The following is a list of the ***manual*** (non-automated) design checks that ***must be made prior to submitting a design to AMCC for the final design review***. AMCC recommends that ***the designer review this list as well as the design rules for the array (Volume II, Section 2) before starting a design***.

These are the essential checks which, if not completed, may delay acceptance of a circuit for production

For any design rule violation or variance, including special macros, a pre-approval request form (a "PAR") must be submitted and approved prior to design submission.[4] The approved PAR (waiver) must be attached to and submitted with the design submission package. Consult AMCC Applications Engineering if you have questions.

> *Every waiver carried the potential for causing design implementation problems. We call these "show stoppers" today.*
>
> ***Note**: This list must be completed., and any additional required pages attached as needed (ERC report, explanations of the resolutions of exceptions, any waivers, etc.), before the design submission package is considered to be complete.*

KEY: Where an automated ERC check is not feasible (usually due to design-dependence), and the check cannot be programmed, the flag [MANUAL] is used.

1.1 Schematic Check – All Technologies

_____ Has the schematic been prepared following the general AMCC rules as defined in Volume II, Section 3, and the EWS-Specific rules listed in Volume II, Section 7 of the appropriate design manual? Check completed items:

_____ Have the macro conventions been followed?

_____ Are all macros named? (Except in a DAISY Hierarchical design)

_____ Have "come from" page notes been included for all schematic page inputs?[5]

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[2] These were the prevalent schematic-capture design systems at hte time.

[3] Today these are the reports generated by the Synthesis tool such as Design Compiler, and by the pre-wafer DRC checks.

[4] Sometimes these could be waived, sometimes not. They usually came with a delay and a fee.

[5] In 40-50-60 and more schematic page designs, it helps to know which page the source signal came from, and where a signal is going..

_____ Have “go to” page notes been included for all schematic page outputs?

_____ Have internal nets been named or default net names been made visible (critical paths, etc.)? (**Note**: If more than 20% of the circuit is involved in critical path timing, consult AMCC.)

_____ Have all internal 3-state enable signals and bidirectional signals been named (and listed in simulation output)?

_____ Are the critical paths highlighted? [6]

_____ Are the AC test paths highlighted?

_____ Have all unresolved ERC errors been documented with an explanation and an AMCC waiver? [MANUAL]

For Information Only:

_____ Is the schematic type:

_____ Flat?

_____ Hierarchical?

_____ Nested? (DAISY)

_____ Other? [_____]

_____ Are signals routed with busses?

1.2 Circuit Characterization – All Technologies

_____ Has the MacroMatrix Installation and User’s Guide been referenced for border information? (Volume II, Section 7)

_____ Has the chip macro been checked to match the desired array, ECL input type, power supply, timing, I/O mode, and product grade?

_____ Was a different product grade (MIL, COM) used to generate the ERCs than was used to generate the annotation files? (i.e., industrial grade circuits)

Explain_____

1.3 Macro Check – All Technologies

_____ Have all of the macros used in the design been approved by AMCC, from an official release or update? [7]

1.4 Simultaneously Switching Outputs – Added Power and Grounds

_____ Has the SWGROUP macro parameter been correctly used on simultaneously switching outputs (SSOs), and the power and ground macros added to accommodate them to allow automated ERC extra power and ground population checks?

_____ No simultaneously switching outputs

TTL outputs are simultaneously switching if they switch within 3ns of each other. ECL outputs are simultaneously switching if they switch within 2ns of each other.

_____ Were the appropriate number of added power and ground (ITPWR, ITGND, IEVCC) macros used for other circuit conditions? [ERC; MANUAL]

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[6] Remember that this was before Design Compiler, edif, RTL, and all of that EDA support.

[7] Believe it or not, this check still applies today to any foundry library.

_____ Are there any unused pads and/or pins available that may be used to improve controllability or observability, or that may be used for extra power and ground for better noise immunity, should AMCC determine that they are needed?

1.5 ECL Checks

_____ Has the correct drive capability been used for the ECL outputs as available for the chosen array? (25, 50 Ohms) [MANUAL]

_____ Has the correct ECL input been used for the intended frequency of operation? [MANUAL]

_____ Has the correct ECL output been used for the intended frequency of operation? [MANUAL]

_____ Has differential ECL output been used then +5V ECL is driving off-board (remote)? [MANUAL]

_____ Are paired differential ECL I/O macros adjacent on the schematic? [MANUAL]

_____ Have the proper macros been used for differential ECL I/O? [MANUAL]

_____ Was the requirement for minimal, balanced loads on the macros driving differently paired ECL output macros honored? [MANUAL]

1.6 TTL I/O Check

_____ Did you review the input requirements on inverting TTL input macros? (See the macro documentation.) [MANUAL]

1.7 Fan-Out Check

_____ Have the clock and distortion-sensitive paths been properly derated using the FOD (fan-out derating) net parameter? [ERC; MANUAL]

_____ Have you followed the guidelines for driving ECL differential pairs as described in Volume I, Section2, Design Methodology, including the use of FOD as required? {ERC, MAUNAL]

1.8 3-State Enable – Bidirectional Enable – 3-State Enable-Driver – Bipolar

_____ Are all internal 3-state and bidirectional enable signals listed in the simulation output file format (in the AMCCSIMFMT files)? [MANUAL]

_____ Can internally-generated 3-state and bidirectional enables be disabled and the enable signal driven externally during test? [MANUAL]

1.9 AMCCIO.LST, AMCCPKG.LST, AMCCANN Check

_____ Were the TTL I/O macros operating above 50MHz identified using the AMCCANN interface?

_____ Were the ECL I/O macros operating above 100MHz identified using the AMCCANN interface?

_____ Were unusual ECL resistive terminations identified using the AMCCANN interface?

_____ Does the system load capacitance shown in AMCCPKG.LST match what was used in the computations of the path dpecification for all paths in the AC tests? (required)

1.10 Power Check – All Technologies

_____ Has the worst-case power computation performed by the ERCs been adjusted for any non-standard conditions (different power supplies; duty-cycle on the ECL outputs; termination values for the ECL outputs; etc.? [MANUAL]

What adjustment? _____

1.11 Master-Slave F/F – All Technologies

_____ Has a common clock been used for the master-slave latch flip/flop implementation? [MANUAL]

_____ Have you taken care not to use any core and I/O macros in combination to build a F/F or complex devices? [MANUAL]

1.12 Package Selection Check – All Technologies

_____ Was the package you intend to use available on the AMCCANN interface menu?

If not, list the intended package: _____

_____ Has the intended package been approved by AMCC?[8] [MANUAL]

_____ Does the sum of all I/O signals plus all fixed and added power and ground pads meet the pin/pad alignment restrictions of the selected array and package combination? [MANUAL]

_____ Has the junction temperature been computed to meet specified array limits of 130^{o}C (COMmercial) or 150^{o}C (MILitary)? [MANUAL]

Computed Maximum Junction Temperature

_____^{o} C for specified system environment

Θ_{ja} _____ Θ_{jc} _____

Max T_{case} _____ ^{o} C Max Ambient _____ ^{o} C

_____ If the junction temperature computed above is too high, has AMCC been consulted on the cooling methodology selected? [MANUAL]

_____ If a heat sink is required, has one been identified and specified? [MANUAL]

_____ Heat Sink chosen

_____ Used in the above junction temperature computation?

1.13 Clock [MANUAL CHECKS] – All Technologies

_____ When selecting macros, did you consider macro selection, macro placement, the design objectives, specification, and maximum frequency requirements?

_____ Have all critical and sensitive paths in a circuit been identified and the critical path timing(s) computed?

_____ Have the critical path propagation delays and the external set-up and hold times been calculated, using worst-case MAXIMUM and MINIMUM conditions, under both rising and falling edge input conditions?[9]

_____ Have these been included in the design submission package?

_____ Are the desired external set-up and hold times specified?

_____ Is the required maximum operating frequency specified?

_____ Is the desired clock frequency within reasonable limits for the array,[10] path depth, macros used, and selected I/O mode?

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[8] One designer didn't do this – made a big mess – a package design takes up to 18 months. Big Whooops!

[9] PrimeTime now does this for you, and yes, it can handle dual libraries (as can Design Analyzer). Check with the specs on synopsys.com.

[10] read process or technology

_____ Have the pulse distortion effects been evaluated and minimized?[11]

_____ Have the toggle rates of the macros used been verified to be within the macro specification limits? L-option macros are especially vulnerable to mis-use.[12]

Q3500 Series (bipolar): When a design will operate the EDL output buffers at speeds ≥ 125MHz; consult AMCC Applications through the AMCC Sales Representative or sales office.

Q5000 Series (bipolar): When a design will operate the EDL output buffers at speeds ≥ 200MHz; consult AMCC Applications through the AMCC Sales Representative or sales office.

1.14 Test / Testability Checks – All Technologies

_____ Have the functional, at-speed, and AC Test simulation vectors been submitted per AMCC requirements? Refer to Vector Submission Rules and Guidelines, Volume II, Section 4.

_____ Have annotation worst-case maximum delay values been used in the maximum worst-case simulation?[13]

_____ Have annotation worst-case minimum delay values been used in the minimum worst-case simulation?

_____ Did you simulate the design for both minimum and maximum worst-case conditions and compare the results for a functional match?

_____ Have you been careful **NOT** to use the Front-Annotation (pre-layout) simulation results as the circuit specification? (***i.e., do not use the front-annotation results as the circuit spec!)***

If yes, consult AMCC.

_____ Has the AMCCVRC (Test Vector Rules Check) software been used to check all AMCCSIMFMT simulation results being submitted for Functional and AC Test? (Only Maximum worst-case sampled files must be checked.)

_____ Have all reported AMCCVRC errors been documented with an explanation? (resets, sets)

_____ Is the sum of the maximum worst-case delay for the longest path in the circuit plus 50ns less than 100ns?

If yes, the sample step for functional and AC test is 100ns.

If no, increase the sample increment to 200ns or 300ns.

_____ Sample increment used in Functional and AC Test simulation in ns.

_____ Has the At-Speed simulation been sampled at least once per the period of the specified maximum operating frequency? (For help in selecting the sample step for At-Speed simulations, consult AMCC Applications.)

_____ Sample increment used in At-Speed simulation in ns.

_____ For functional, at-speed, and AC test simulations, have any of the AMCCSIMFMT simulation output files been edited? (This does not refer to a copy made of the file for the purpose of editing the file, but to the original file itself. If a copy was made, submit both the edited and unedited copy.) [14]

If yes (original file was edited), re-run for a clean copy.

_____ Do all submitted functional, at-speed, and AC test simulations use the same signal format (I/O ordering)? (In other words, are all the files in the same readable format so someone can easily move from one to another?)

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[11] Jitter, uncertainty

[12] Pulse-swallowing can occur if this is violated

[13] You would be surprised-----

[14] These days, vector files can have comments embedded in them. In fact, they had better!

_____ Have any additional tests, (bench, etc.) been requested with written instructions per AMCC requirements? [15]

_____ Regardless of the EWS capabilities, has binary been used as the numeric base in all AMCCSIMFMT file?

_____ Have race and hazard conditions in the design been checked for using the at-speed simulation and timing checks? VALID systems: at-speed or timing verifier checks?

_____ Has fault-grading been performed?

_____ Result included

_____ AMCC to do this

If result included, what fault-grading software was used? _____

_____ If fault-grading (vector analysis) has been performed, has 90% coverage been obtained?[16]

_____ Fault-Grading score

_____ Optional: Has testability analysis (hardware design) been performed?

_____ Result included

_____ Have all timing check reported errors been documented with an explanation and an AMCC waiver?

_____Number of vectors submitted:

_____ Functional

_____ At-Speed

_____ AC Test

1.15 Preplacement Request Check – All Technologies

_____ Has any pre-placement been requested or a pre-placement file been included in the design submission package?

_____ Has any such file been developed according to the rules and guidelines in the AMCC Placement Guide?

[15] This is NOT a test bench as it applies today

[16] These days, 98% or better preferred